Karunya University
(Karunya Institute of Technology and Sciences)
(Declared as Deemed to be University under Sec.3 of the UGC Act, 1965)

End Semester Examinations - 2015-16 Even Semester - May 2016

14EC3054 Hardware Design Verification Techniques

Set B

Time : 3 hrs
Total Marks: 100

1. (i) Explain in detail about Event Driven Simulation.(10)

   (ii) If the portion of a design do not meet the requirements for cycle-based simulation ,how the simulation is proceed further. (10)

OR

2. (i) How to check the correctness of Verilog and VHDL Source code using Linting Tools?(12)

   (ii) Discuss about stimulus and response. (8)

3. (i) What is first-time success, how a design is verified, and which test benches are written-Discuss in detail about the verification plan.(14)

   (ii) With neat source code discuss in detail about Statement Coverage. (6)

OR

4. (i) Explain in detail about third party models. (5)

   (ii) Explain the most common verification tools used in conjunction with simulators.(10)

   (iii) Discuss about Grapevine System. (5)

5. (i) All design teams have informal systems to track issues and ensure their resolutions. Find the issues and check the functionality of the design. (14)

   (ii) The application of synchronous data can be encapsulated. With neat waveform and source code explain in detail about the condition described above.(6)

OR

6. (i) The test bench approach requires a similar configuration of the design, use the same abstraction level for the stimulus and response.Determine the appropriate test bench approach. (6)

   (ii)Using test vectors,verifying a design is cumbersome and they are hard to interpret and difficult to specify correctly.Find a suitable method for the design to verify it and observing the response.(14)

7. (i) How a zero delay and Non-zero delay waveforms are generated in Synchronous circuits? (8)

   (ii) Explain in detail about Verification.(12)

OR

8. (i) All design teams have informal systems to track issues and ensure their resolutions. Find the issues and check the functionality of the design.(15)

   (ii) Write in detail about features to testcases.(5)

9. (i) Explain in detail about Combining eVCs and give its uses.(12)

   (ii) Describe briefly Reusable Verification Components(eVCs),Clocks ,Events,DUT Signals and Agent Details. (8)